

CLAIMS

A method comprising: 1.

receiving an input clock *signal representing either a differential clock signal or # single-ended clock signal; determining whether the |input clock signal is a differential clock signal of a single-ended clock signal;

and

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automatically generat#ng an output clock signal based

on the determination.

The method of claim 1 wherein generating the output 2. 1

clock signal comprises generating a single-ended output 2

clock signal when the imput clock signal is determined to 3

be a differential clock signal.

The method of claim 1 wherein the generated clock 1

signal has the same #requency as the input clock signal.

The method of claim $1/\sqrt{}$ wherein receiving the input

clock signal comprises refeiving a single-ended clock

signal on a first input /terminal and a ground potential on

the second input terminal.

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The method of claim 1 further comprising generating a clock mode signal based on the determination.

6. A method comprising:

receiving a first input clock signal;

receiving a second input clock signal, wherein the second input clock signal is one of a constant signal at

5 ground potential, a constant signal above ground potential

6 or a signal at the same frequency as the first input clock

7 signal;

automatically generating a single-ended clock signal

9 from the first and second input clock signals when the

10 second input clock signal is one of a constant signal above

ground potential or a signal at the same frequency as the

12 first input clock signal; and

automatically generating a single-ended clock signal

14 from the first input clock signal when the second input

15 clock signal is a constant signal at ground potential.

The method of claim wherein the output clock signal is a single-ended clock signal generated when the input clock signal is determined to be a differential clock signal.

The method of claim wherein the generated clock signal has the same frequency as either as the first input clock signal or the second input clock signal.

1 9. A device comprising:

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a first terminal to receive a first clock input signal;

a second terminal to receive a second clock input

5 signal; and

a detector coupled to the second terminal to receive

7 the second clock input signal, wherein the detector is

8 configured to output a clock mode signal as a function of a

9 voltage potential of the second clock signal.

1 10. The device of claim 9 further comprising:

a first circuit coupled to the first terminal

3 configured to generate a first single-ended clock signal of

4 the same frequency as the first clock input signal;

a second circuit coupled to the first terminal and to

6 the second terminal to generate a second single-ended clock

7 signal of the same frequency as the first clock input

8 signal; and



- a selector configured to select the first single-ended 9
- clock signal or the second single-ended clock signal based 10
- upon the clock mode signal. 11
- The device of claim 10 further comprising a clock
- generator coupled at least to the first terminal,
- configured to output a master c#ock signal.
- 12. The device of claim 11, further comprising a
- compensator configured to receive the signal from either
- the first circuit or the second circuit and to output a
- core clock signal aligned with the master clock signal.
- The device of claim 12 wherein the compensator
- includes a phase-locked loop. 2
- The device of claim 12 wherein the compensator 1
- includes delay cancellation as a function of the clock mode 2
- signal. 3

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- The devi/ce of claim 10 wherein the selector is a
- multiplexer,
- comprising:

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a switch including an input terminal and an output
terminal;
load coupled to the output terminal; and
a capacitor coupled to the output terminal;
wherein the input terminal receives a periodic clock
signal; and
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wherein the capacitor is so sized to filter out pulses

9 caused by the oscillations of the clock signal applied to

10 the input terminal of the switch.

1 17. The device of claim 16, further comprising an output

2 buffer coupled to the output terminal.

1 18. The device of claim 16, wherein the switch comprises a

2 field effect transastor and the input terminal comprises

3 the gate of the field effect transistor.

1 19. The device of claim 16, wherein the switch transistor

2 and the load are CMOS transistors.

. A method comprising:

receiving an input clock signal representing either a differential clock signal of a single-ended clock signal;

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- determining whether the input clock signal is a
- 5 differential clock signal or a single-enged clock signal;
- 6 and
- automatically generating a clock mode signal based on
- 8 the determination.
- 2 providing a first circuit for a single-ended clock
- $_3$ signal, the output of the first $q_{
 m i}^{
 m l}$ rcuit being a first
- 4 output clock signal;
- providing a second circuit for a differential clock
- 6 signal, the output of the second circuit being a second
- 7 output clock signal;
- selecting either the output of the first circuit or
- 9 the output of the second circuit as a function of the clock
- 10 mode signal.
- 1 2/2. A method comprising:
- receiving a first periodic clock signal voltage at a
- 3 first input;
- receiving at a second input one of a second periodic
- 5 clock signal voltage, a constant signal voltage above
- 6 ground potential or a constant ground potential signal;



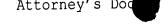
- detecting whether the signal receifed at the second 7
- input is a constant ground potential #signal; and
- generating a clock mode signal indicative of the
- detection. 10

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- The method of claim 1/2 further comprising generating a
- high voltage clock mode signal when the signal received at
- the second input is a constant ground potential signal.

24. A method comprising: 1

- receiving a clock signal, wherein the clock signal is
- one of a single-ended clock signal or a differential clock
- signal; and
- generating an output single-ended clock signal that 5
- follows the received clock signal.
- The method of claim 24 further comprising aligning the 1
- output single-ended clock signal with the received clock 2
- signal. 3
- A system comprising: 26. 1
- a clock generator, wherein the clock generator issues
- one of a single-ended clock signal or a differential clock
- signal; and



- an electronic device including a first input terminal 5
- and a second input terminal, with the first input terminal
- coupled to the clock generator;
- wherein the electronic device generates a single-ended
- clock signal of the same frequency as the clock signal
- issued by the clock generator. 10
- 27. The system of claim 26, wherein the electronic device
 - issues a single-ended clock signal aligned with the clock
- signal issued by the clock generator.
- 28. The system of claim 26,
- wherein the electronic device includes a first input
- terminal and a second input terminal, and
- wherein the first input terminal is coupled to circuit 4
- ground when the clock generator issues a single-ended clock
- signal.
- 29. The system of claim 26,
- wherein the electronic device includes a first input 2
- terminal and a second input terminal, and 3
- wherein the first and second input terminals are 4
- coupled to the clock generator when the clock generator
- issues a differential clock signa.